# Extraction of SPICE Model for Double Gate Vertical MOSFET

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## Abstract

*Vertical MOSFETs device have one important disadvantage, which is higher overlap capacitances such as the separated gate-source and gate-drain parasitic capacitances ($C_{GSO}$ and $C_{GDO}$), which is known to be most crucial to the high-frequency/speed performance but very hard to extract. In this paper presents parameter extraction techniques to create an extended BSIM model card of vertical p-MOSFETs for circuit simulation with SPICE can be accurately obtained for these overlap capacitances determination.*

*This device was modeled as a subcircuit with any sub elements such as resistors, capacitors and diodes that capture the parasitic effects. The subcircuit was simplified in order to modeling in BSIM easily. The overlap capacitances of vertical p-MOSFET can be determined by using capacitance parameter extraction of quasi static small signal equivalent circuit. The result showed that gate-drain paracitic capacitance ($C_{GDO}$) is larger than gate-source parasitic capacitance ($C_{GSO}$)*

## 1. Introduction

A vertical MOSFET is structure with promising performance to replace mainstream lateral devices for reducing the channel length of transistors under 50 nm. First, the channel length is defined using techniques other than lithography, for example epitaxy or ion implantation. Lithography has to be used to achieve a small memory area or a short channel length, because these are defined sublithographically by layer thicknesses and etching. Second, self-aligned double and surround gates can readily be realised with easy access to the gates. Third with surround gates, vertical MOSFETs offer increased current drive per unit silicon area [1-3].

The Vertical MOSFET with Double Gate structure is recognized to be the most scalable MOSFET for its high short-channel effect (SCE) immunity. In addition, independent DG-MOSFET has great advantage to enable the threshold voltage control for the flexible power management.

One of the main problems inherent to the vertical layout is a large overlap capacitance between the gate track and the source-drain electrodes, which are only separated by a thin gate oxide. The contact to the surround gate is created via a polysilicon track that overlaps onto the top of the pillar. The large overlap of polysilicon gate surrounding the drain and source regions of the mesa leads to very high overlap capacitances.

Moreover, it is very important to accurately extract the gate resistance because the gate resistance affects the current-gain cutoff frequency ($f_T$), the maximum oscillation frequency ($f_{max}$), the input-referred thermal noise, and the time response to the modulation of the input signal in the gate [4,5]. Therefore extraction of model for optimised devices need be done. The device extraction modeling was performed on the same electric parameter and the same devices under TCAD Simulator to minimise the influence of process deviations.

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## 2. Physics device model

The channel region of Double-gate Vertical MOSFET is surrounded by two gates in parallel [6]. Each of these two gates generates an inversion layer. If the silicon is thin enough, these two inversion layers overlap, so the whole channel region is inverted. By this, the field under the gate is altered favorably in a way, that the field does not penetrate the channel from drain to source, so DIBL and threshold roll-off are suppressed. Furthermore, calculations show that double-gate MOSFETs should show almost ideal sub-threshold behavior [7].

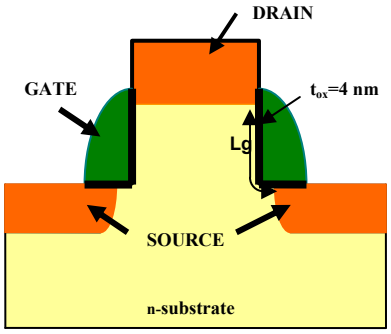



Figure 1. Double gate vertical p-MOSFET structure layout

In a Double-Gate MOSFET the silicon channel layer is only a few tenth of nm thick and on both sides there is a gate stack. These two gates are biased in parallel to form an inversion channel on both sides of the silicon. If the silicon layer is thin enough, these two inversion channels will overlap. By means of this, the field penetration from drain to source is decreased, which decreases short channel effects [9].

The double-gate operation allows the second gate to affect the charge density at the surface under consideration. Modifications to the bulk formulation to include the second gate effect have to be incorporated. In our present formulation, the currents of at the 2 interfaces are calculated separately and add together. The drain current at one of the interfaces is given by:

$$I_{DS} = \mu_{eff} W_{qI} \frac{dV_{ch}}{dy} \qquad (1)$$

where qI is the normalized inversion charge given by $Q_{inv}/(C_{ox}v_{th})$ where the $Q_{inv}$ is the inversion charge and vth the thermal voltage. All the voltages are also normalized by the thermal voltage vth for simplicity. $V_{ch}$ is the quasi-Fermi potential in the channel and current flows in the positive y direction. The inversion charge in the channel can also be expressed by

$$q_I(y) = q_{I0} \exp\left[\frac{\phi_s(y) - V_{ch}(y)}{V_{th}}\right] \qquad (2)$$

Differentiating (2) and rearranging gives

$$\frac{dq_I}{q_I} = d\phi_s - dV_{ch} \qquad (3)$$

Considering the gate to channel direction, and assuming linearization between the gate voltage and surface potential, the normalized inversion charge can be calculated in the same way as in bulk MOSFETs:

$$dq_I = \partial V_{G1} + \rho \partial V_{G2} - n_1 d\phi_s \qquad (4)$$

Notice that the inversion charge is modulated by both front and back gate voltages. In the bulk case, the effect of $V_{G2}$ is mimicked by the body voltage, which is incorporated into the threshold voltage, taking the body voltage as a reference. Due to the DG model of operation that also requires symmetry between the 2 gates, the dependent of inversion charge on both gate voltages have to be expressed explicitly. $n_1$ is the ideality factor of the first interface and is different from that of bulk MOSFET. Its value is given by

$$\frac{dq_I}{q_I} + \frac{dq_I}{n_I} = \frac{\partial V_{G1}}{n_1} + \frac{(n_1 - 1)\partial V_{G2}}{n_1} - dV_{ch} \qquad (5)$$

Considering the current at a given gate voltages, (5) and (1) can be combined to eliminate the quasi-Fermi potential ($V_{ch}$). An expression of current in term of charge is obtained.

$$I_{DS} = \mu_{eff} W_{qI} \frac{(1 + q_I / n_1) dq_I}{dy} \qquad (6)$$

Integrating (6) from source to drain, the drain current is then explicitly given by:

$$I_{DS} = \frac{\mu_{eff} W}{L}\left[\frac{q_S^2 - q_D^2}{2n_1} + (q_S - q_D)\right] \qquad (7)$$

where $q_S$ and $q_D$ are the normalized charge at the source and drain respectively. To solve for $q_S$ and $q_D$, (5) is integrated giving:

$$\ln\left(\frac{q_I}{n_1}\right) + \frac{q_I}{n_1} = \left(\frac{(V_{G1} + (n_1 - 1)V_{G2} - V_{T1}}{n_1} - V_{ch}\right) \qquad (8)$$

where $V_T$ is obtained from the integration constant. Equation (8) is the diox equation with an analytical solution of

$$q_I = n_1 \ln\left[1 + \exp\left(\frac{(V_{G1} + (n_1 - 1)V_{G2} - V_{T1}}{n_1} - V_{ch}\right)\right] \qquad (9)$$

by replacing $V_{ch}$ by the S/D voltage, $q_S$ and $q_D$ can be evaluated. [10]

## 3. Parameter Extraction Optimisation

The double gate vertical p-MOSFET that is showed at figure 1 can be modeled be subcircuit model (figure 2a). The key electrical parameters are be set to same condition. The IC simulator computation of low frequency transconductance $g_m$, and output conductivity $g_{DS}$ is done from the I(V)characteristics. Thus the basis for the following capacitance and RF-parameter extractions is given by these DC-parameter extraction results.

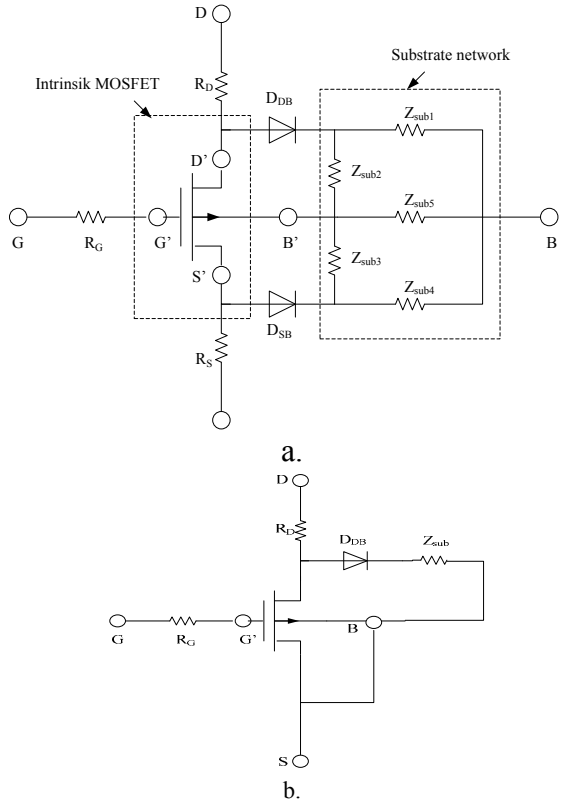



Figure 2. Subcircuit of vertical p-MOSFET model
a. Subcircuit model inclusing paracitics
b. Simplified subcircuit model

Under circuit simulation of BSIM model card with SPICE and TCAD simulation, I-V curve of this device subcircuit is described at Figure 3 below. In order to comparison of I-V characteristics between the simulated and modeling DC characteristics in Figure 3 achieve a good fitting is by a set of DC-parameters was extracted by means of a suitable application of original BSlM3v3 'local optimisation strategy'. The model parameter of double gate vertical p-MOSFET can be obtained as table 1 below.

Table 1. Key device parameter

| | |
|---|---|
| $V_{DS}$ (V) | -2.5 |
| $V_{GS}$ (V) | -1.5 |
| L (μm) | 0.13 |
| $d_{ox}$ (nm) | 4 |
| Sb (mV/dec) | 75 |
| $V_{th}$ (V) | 0.5 |
| $g_m$ (μS/μm) | 254 |
| $G_{DS}$ (μS/μm) | 68 |
| $h_{21}$ (GHz) | 4 |
| $f_T$ (GHz) | 2.8 |
| $f_{max}$ (GHz) | 2.6 |

The design of the devices for testing does not allow bulk biasing. Problems concerning DC-modelling vertical MOSFETs are short channel effects and a possible appearance of the floating-body effect. Figure 3 displays no kink effect in the I(V) curves.

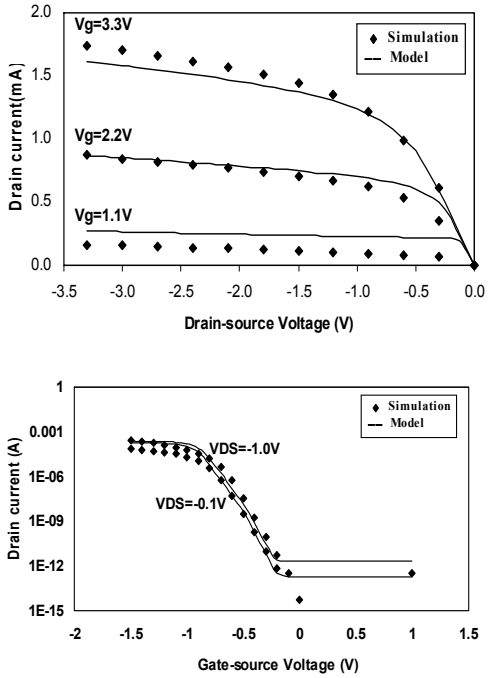
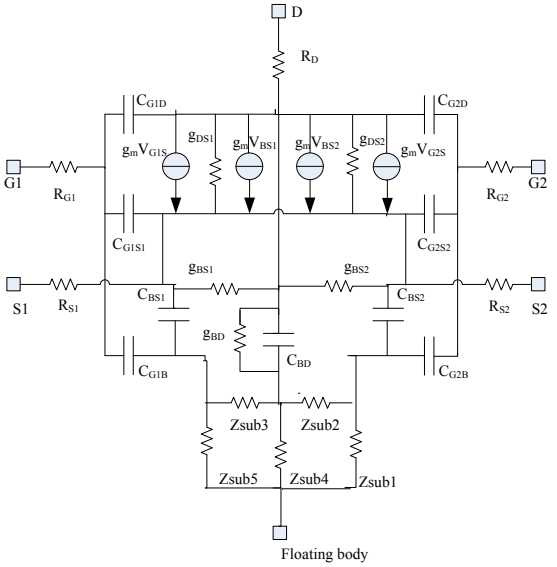



Fig. 3. I-V characterisation of device with L=0.13μm W=5 μm

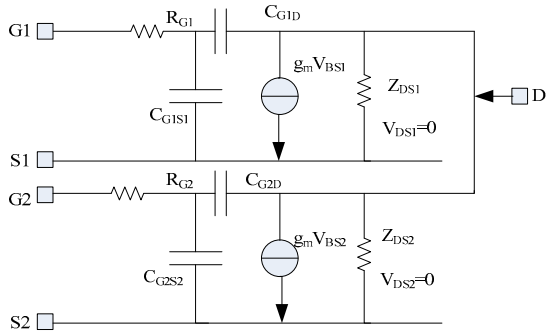
## 4. Capacitance parameter extractions

The device structure of double gate vertical MOSFET (Figure 1) can be assumed as equivalent circuit that can be pictured at Figure 4a. The vertical MOSFET has no bulk contact. This leads to more complicated test structures for C(V) measurements to determine overlap and fringing capacitance parameters as for lateral MOSFETs. Simplified of this circuit can

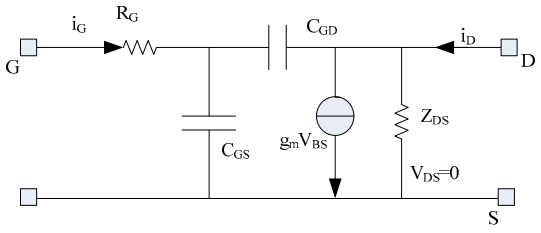
be performed as figure 4b. In our case, the device is symmetrical double gate device, where both gates ($G_1$ and $G_2$) are connected be one gate (G) and both sources ($S_1$ and $S_2$) are connected be one source (S), so that the connection can be combined with calculate as parallel circuit formula. This circuit can be simplified again became circuit as be showed at Figure 4c.




a.




b.




c.

Figure 4. Equivalent circuit
a. Double gate Vertical MOSFET Equivalent circuit
b. Simplified equivalent circuit
c. Simplified symetrical device equivalent circuit

where total resistances (R) and capacitance (C) of gate (G) and source (S) are

$$C_{GD} = C_{G1D} + C_{G2D} \quad (10)$$

$$C_{GS} = C_{G1S1} + C_{G2S2} \quad (11)$$

$$Z_{DS} = \frac{Z_{DS1}.Z_{DS2}}{Z_{DS1} + Z_{DS2}} \quad (12)$$

The sidewall junction capacitance could not be specified due to the vertical geometry of the junctions. The bottom junction capacitance can he described as

$$C_j(V) = CJ(1 + V/PB)^{-MJ} A \quad (13)$$

where CJ is the bottom junction capacitance per unit area at zero bias, PB the diffusion voltage, MJ the grading coefficient, and A the junction area. These BSIM parameters were therefore extracted from C(V) measurements at large area test structures, as illustrated in Fig. 3. In a first step the overlap capacitances were estimated from the geometrical structure with the simple capacitor formula

$$C_{ov} = \varepsilon_{ox} l_{ov} W / d_{ov} \quad (14)$$

where lov is the length of the source or drain overlap under the gate. $C_{ov}$ was normalised to the gate width W. and implemented as $C_{GDO}$ and $C_{GSO}$ into the model card.

Due to the unsymmetrical device structure these calculations have to be made for source and drain overlaps separately. The outer fringing capacitance (the corresponding BSIM-parameter is $C_F$) was also determined from the geometrical device structure and can be expressed as

$$C_{of} = \frac{2}{\pi} \varepsilon_{ox} W \ln\left(1 + \frac{t_{gate}}{d_{\alpha}}\right) \quad (15)$$

where $t_{gate}$ is the height of the poly-gate edge.

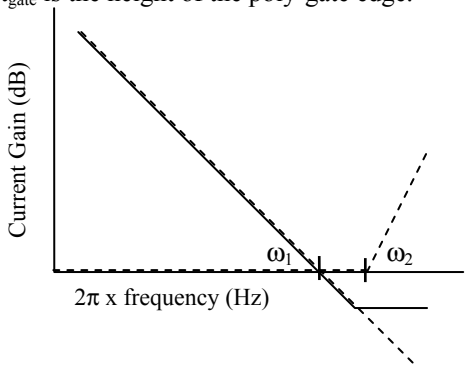



Figure 5. $h_{21}$ graph for extraction of $C_{GDO}$ and $C_{GSO}$

The inner fringing capacitance $C_{if}$ was neglected because BSIM cannot handle the case when shielding effects appear at inversion layer formation ($V_{GS}>V_{th}$)

Thus, start values for the capacitance parameters were determined, and optimised, in a second step, by the following methodology. Note that $C_F$, $C_{GSO}$ and $C_{GDO}$ are part of $C_{GS}$ and $C_{GD}$.

The detailed small-signal equivalent circuit is displayed in Fig. 4 and was simplified for the use of the compact model, as shown in Fig. 4c. The small-signal current gain were defined as $i_D$ over $i_G$ with shorted output:

$$h_{21}(j\omega) = \left.\frac{i_D}{i_G}\right|_{v_{DS}=0} = \frac{v_{GS} g_m - v_{GS} j\omega C_{GD}}{v_{GS} j\omega [C_{GS} + C_{GD}]} \quad (16)$$

$$h_{21}(j\omega) = \frac{1 - j\omega/\omega_2}{j\omega/\omega_1} = \frac{h_2(j\omega)}{h_1(j\omega)} \quad (17)$$

The replacement of $i_D$ and $i_G$ with the small-signal parameters $g_m$, $C_{GS}$, $C_{GD}$ in (4) and a simplification of these terms leads to the ratio of two transfer functions

$$h_1(j\omega) = j\omega/\omega_1 \quad (18)$$

$$h_2(j\omega) = 1 - j\omega/\omega_2 \quad (19)$$

$h_2$ over $h_1$ corresponds to the addition of $1/h_1$, and $h_2$ magnitudes in decibels, as displayed in Fig. 5. The shape of $h_{21}$ has two characteristic frequencies:

$$\omega_1 = 2\pi f_T = g_m/[C_{GS} + C_{GD}] \quad (20)$$

$$\omega_2 = g_m/C_{GD} \quad (21)$$

where $f_T$ corresponds to the extrinsic transit frequency. The simulation $h_{21}$-data within the complete frequency range can be showed at Figure 6 below.

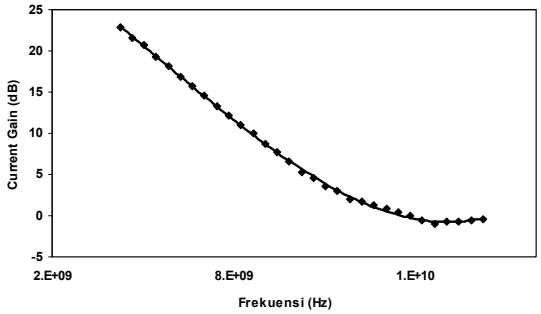



Figure 6. h21 graph result of double gate vertical p-MOSFET

The graph can determine gate-drain paracitic capacitance ($C_{GDO}$) is larger than gate-source parasitic capacitance ($C_{GSO}$) using curve fitting as explain at Figure 5. The calculation of these overlap capacitance use equation (20) and (21). The result are $C_{GDO}$= 12.34 nF/m and $C_{GSO}$= 4.67 nF/m. These result shows that $C_{GDO}$ is larger than $C_{GSO}$ because interface area of gate-drain is greater wider than gate-source

## 4. Conclusion

The parameter extraction technique to determine create overlap capacitance of double gate vertical p-MOSFET is presented very well by using BSIMDG model card with SPICE. This device was modeled as a subcircuit with any sub elements such as resistors, capacitors and diodes that capture the parasitic effects. The subcircuit was simplified in order to modeling in BSIMDG easily. It is optimised from I(V)curves for similar of key device parameter and geometry between TCAD simulation and modeling until shows a good agreement DC characteristics. The model parameters can be obtained from this extraction. The overlap capacitances of vertical p-MOSFET can be determined by using capacitance parameter extraction of quasi static small signal equivalent circuit. The result showed that gate-drain paracitic capacitance ($C_{GDO}$) is larger than gate-source parasitic capacitance ($C_{GSO}$)

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