Short Channel Effect of SOI Vertical Sidewall MOSFET

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Abstract **Application of asymmetric sidewall vertical metal oxide semiconductor field effect transistors (MOSFETs) is hindered by the parasitic overlap capacitance associated with their layout, which is considerably larger than for a lateral MOSFET on the same technology node. A simple process simulation has been developed to reduce the parasitic overlap capacitance in the asymmetric sidewalls vertical MOSFETs by using SOI (Silicon on Insulator) in bottom planar surfaces side. The result shows that while channel length decreases, the threshold voltage goes lower, the DIBL rises and subthreshold swing tends to decrease, for both structures. It is noted that the SVS MOSFET structure generally have better performance in SCE control compared to bulk vertical MOSFET. The presence of buried oxide is believed to increase the performance of vertical MOSFET, essentially in controlling the depletion in subthreshold voltage.**

Index: Sidewall, SOI, parasitic capacitance, vertical MOSFETs.

I. INTRODUCTION

Dimensions of MOSFET are continually scaled to be smaller to improve performance and package density. This down scaling makes structure of MOSFET must be modified that it needs solve include the lithography to achieve reproducibly fine dimensions, source and drain engineering to reduce device parasitic and channel engineering to control short-channel effects.

Vertical MOSFETs are structures with promising performance to replace mainstream lateral devices. A vertical transistor technology would raise the package density, could avoid the lithography problem for the gate layer, and open new ways for optimizing the doping profile using epitaxial layers deposited with atomic layer thickness control and various doping concentrations. One of some vertical MOSFET structures is an asymmetric sidewall vertical MOSFETs, that has a simpler process [1].

There are some advantages of vertical MOSFET. First, the channel length of the vertical MOS transistor is not defined by lithography. Second, vertical MOS transistors are easily made with both front gate and back gate. Third advantage of the vertical MOSFET is the possibility to prevent short channel effects from dominating the transistor by adding processes, such as a SOI to reduce parasitic bipolar effects or a dielectric pocket to reduce drain induced barrier lowering (DIBL). [2-5] The reduction of overlap capacitance of the gate with drain, source and body regions is a recurring theme in recent research. However, several approaches have been proposed to reduce overlap capacitance in vertical MOS devices, including selective epitaxy [6], replacement gate [7] and fillet local oxidation (FILOX) [8].

In this paper, an asymmetric sidewall vertical transistor using Silicon on Insulator (SOI) formation will be proposed. With addition of SOI, this structure tries to reduce the high parasitic capacitance that emerges especially for the gate to bottom electrode capacitance in ion implanted vertical MOSFETs.

II. DEVICE STRUCTURES AND SIMULATION

For comparison and performance evaluation, two transistor structures have been designed: Asymmetric Vertical Sidewall MOSFET without SOI (Fig. 1a.) and with SOI (Fig. 1b.). Figure 1a. represents an asymmetric sidewall vertical transistor with a simpler process that has been introduced in [1]. This device defines source and drain by ion implantation. The layout of transistor is highly compatible with planar devices. Such a device is especially attractive as the cell transistor in a memory,

because the channel can be made long for good off characteristics without consuming too much area [9,10]. Moreover a bulk contact is available which prevents floating body effects. Like planar transistors the devices achieve high transconductance values due to the sub lithographic definition of the channel length. However, this device have one important disadvantage, which is higher overlap capacitances than conventional lateral devices, which has made them less competitive compared with their lateral counterpart. Overlap capacitances are determined on transistors and gates fabricated with the SOI formation process and compared with values on comparable without the SOI formation transistors. It is shown that a vertical, with SOI architecture gives a lower gate/source overlap capacitance than obtained in comparable device without SOI. Figure 1b. shows the asymmetric sidewall vertical transistor design including the SOI concepts which device structures and simulation of the proposed asymmetric NMOSFET are as follows.

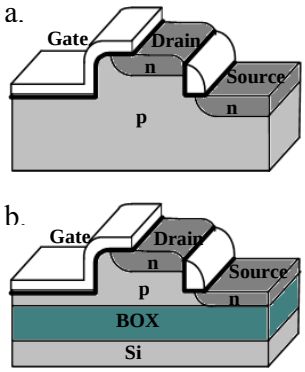

Fig. 1. Asymmetric Vertical MOSFET structures layout (a) Without SOI (b) With SOI

An asymmetric vertical MOSFET with SOI process were simulated using the Atlas Silvaco TCAD simulator. The process uses silicon-on insulator wafer configuration. Boron-doped (9×10^{17} cm^{-3}) wafers (100) served as the starting material. The process flow for the fabrication of the devices is presented in Fig. 2. The first step, after the field isolation a 20-nm thick Nitride layer is deposited, using a lithography mask to define the vertical island by anisotropic dry etching with deep control etching to create 20 nm silicon thickness (t_{si}) outside the silicon pillar area, as shown in fig. 2a. The heights of pillar (133 to 160 nm) were chosen to provide final channel lengths in the range of 50 nm to 125 nm. Next, nitride mask is removed (Fig. 2b), after that gate oxide is grown on the vertical sidewall. The thickness of the final gate oxide is 3 nm (950 °C, 1 min, dry O_2). Then, a 40 nm thick poly-Si film is deposited and patterned by a plasma etching technology to form the gate electrode (Fig. 2c). Following the source and drain areas were implanted with arsenic at a dose of 1.10^{15} cm^{-3} and energy of 35keV, the device is as shown in figure 2d. The next step is to create the smart contact between the source and the body. To begin with, a passivation layer is deposited. Using lithography, we then etch the source/body and source/drain contacts. Once metallization is applied, the asymmetric vertical MOSFET with SOI is complete.

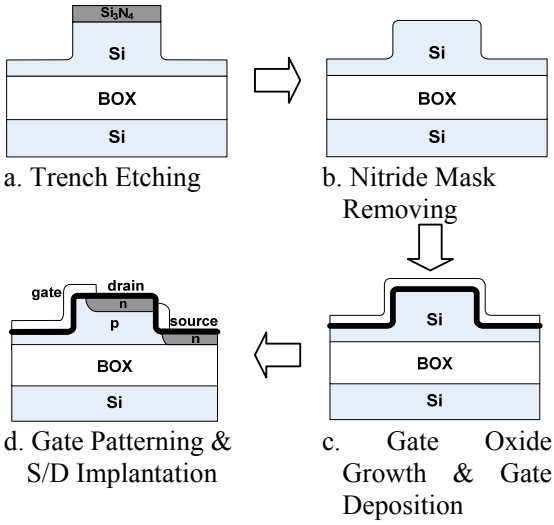

Fig. 2. Process flow for the SOI vertical sidewall MOSFET.

Simulation of the asymmetric vertical sidewall SOI MOSFET will be proposed with its advantages such as control junction leakage and thereby suppress SCEs. Therefore the advantage of the proposed an SOI Vertical Sidewall MOSFET is outlined and associated with fabrication process.

III. RESULTS AND DISCUSSION

By the comparison of Vertical Sidewall MOSFET with and without SOI, figure 3-6 show different result for both structures. The output characteristics of the examined structures are shown in Fig. 3. In this graph illustrates the output characteristic of the device values of gate voltage and demonstrates the expected behaviour.

Device with SOI has a higher saturation current than device without SOI.

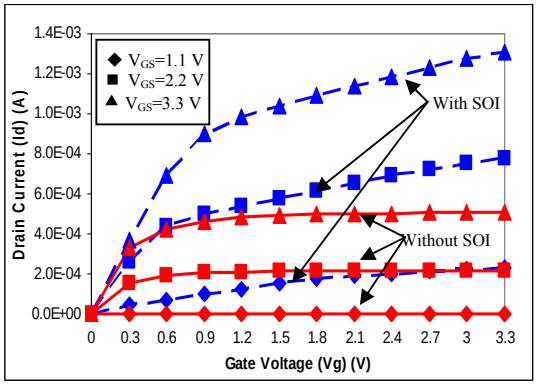

Fig. 3. Id – Vd Characteristics Graph with Lg=75 nm

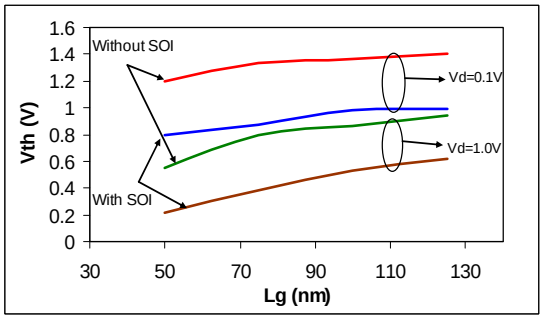

Fig. 4. Threshold Voltage (Vth) Graph of device for Vd=0.1 V and 1.0 V

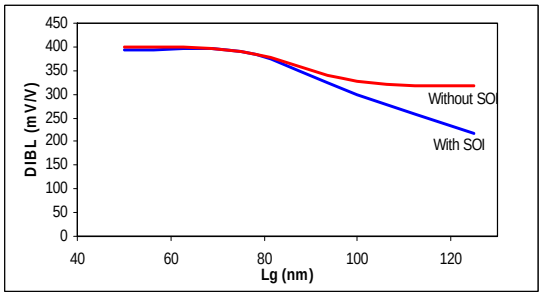

Fig. 5. DIBL Graph

For similar concentration and other parameters of both structures, fig. 4 shows device with SOI has a slightly larger threshold voltage and fig. 5 shows also a slightly higher DIBL compared to device without SOI.

The buried oxide (BOX) of device will be less charge sharing within the region controlled by the source and it also implies that the depletion region controlled by the gate will be larger. This phenomenon is especially significant in short channel devices, where it is found to improve the threshold roll-off of the SOI VSMOS in comparison to the VSMOS without SOI.

The threshold voltage of SOI VSMOS is smaller than VSMOS without SOI. It is suppose that the great threshold voltage degradation is caused by coupling between source and gate makes device much more sensitive to BOX charge trapping so that contribute to V_{th} reduction.

The DIBL of device without SOI is lower because at device with SOI, suppressing SCEs by SOI region that confined between gate oxide and BOX therefore reducing the encroachment of the drain's electric field. If channel length of device is small (for 50 nm and 75 nm), DIBL of device with SOI is smaller than device without SOI although both device are very close.

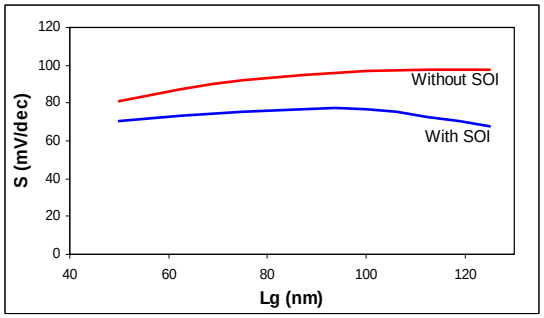

Fig. 6. Subthreshold Slope Graph

Figure 6 depicts comparison on subthreshold slope (S) at various channel length between device with and without SOI. Subthreshold slope (S) is determined by the ratio between oxide capacitance (C_{ox}) and the equivalent depletion region capacitance (C_{dm}). The C_{ox} is determined by the t_{OX}. The SOI can improve its controllability of the channel depletion region thereby causing excellent subthreshold swing so that can reduce C_{dm}. The C_{dm} of structure with SOI is less than without SOI because the C_{dm} is mostly determined by the peripheral capacitive component of the silicon body at device with SOI.

The C_{dm} result for these both structures is shown in the C-V characteristics figure (fig. 7 & 8) below. The structure with SOI is less then without SOI for both configuration: Source-Gate (bottom electrode) as well as Drain-Gate (top electrode) because that the C_{dm} is mostly determined by the peripheral capacitive component of the silicon body at device with SOI

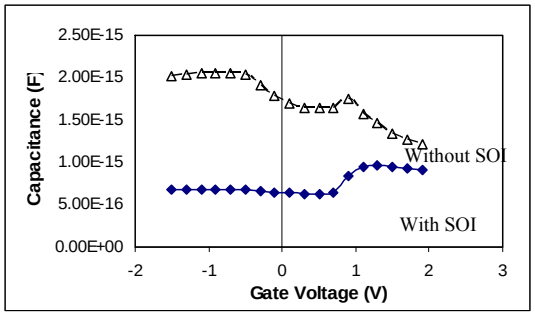

Fig. 7. C-V Characteristic of Source-Gate Graph

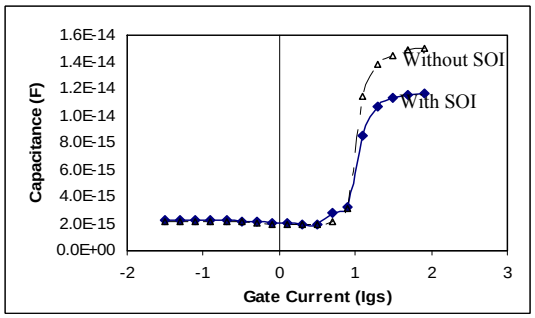

Fig. 8. C-V Characteristic of Drain-Gate Graph

Thus the SOI process allows to fabricate vertical sidewall MOSFETs with overlap capacitance values much lower than the traditional vertical devices and similar to the lateral technology.

IV. CONCLUSION

The simulations and experimental results presented here illustrate the successful implementation of a technique for an asymmetric vertical MOSFET with SOI. The study has suggested that the vertical MOSFETs with SOI provide better SCEs compared to the junction leakage control devices. It uses asymmetric gate configuration, drain-on-top structure fabricated on SOI wafer with substrate thickness of 20 nm over buried oxide. The source junction depth reached all substrate thickness. This structure was compared with bulk vertical MOSFET, both of which were implanted with arsenic of 1.10^{15} cm^{-2}, 35 keV, while the substrate concentration was 9.10^{17} cm^{-3}, boron-doped. Some channel lengths from 125 – 50 nm were compared and analyzed.

The result shows that while channel length decreases, the threshold voltage goes lower, the DIBL rises and subthreshold swing tends to decrease, for both structures. It is noted that the SVS MOSFET structure generally have better performance in SCE control compared to bulk vertical MOSFET. The presence of buried oxide is believed to increase the performance of vertical MOSFET, essentially in controlling the depletion in subthreshold voltage.

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