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ANALYTICAL MODELING OF NON PLANAR MOSFET

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Abstract

The Non Planar MOSFET structure with curved-channel is one alternative MOSFET structure for enhance the electrical performance. The study was focused on the non planar devices which has curved-channel including grooved-gate, recessed-channel, V-shaped and sidewall vertical MOSFET. The presence of corner region can effective in reducing the electric field at the drain, thus improving reliability of short channel effects (SCEs). The corner effect can reduce surface potential. It can improve the characteristic of the device electrical performance, especially the reduction of short channel effect and hot carrier effects. Therefore, the curved-channel MOSFET has a very great application prospect in deep submicron device architecture.
Keywords*: MOSFET, Non Planar, curve channel, surface potential, short channel effects*

Abstrak

MOSFET berstruktur bukan planar terutama bentuk kanal membelok merupakan salah satu alternative MOSFET untuk meningkatkan kinerja listrik divais. Studi ini difoluskan pada divais yang berbelok seperti MOSFET dengan kanal berbentuk lembah dangkal (grooved gate),lembah dangkal (recessed-channel), huruf V (V-shaped) dan kanal vertical berbelok (sidewall vertical) Keberadaan daerah pojok dapat menguranggi medan listrik pada drain serta mengurangi efek kanal pojok. Efek tersebut dapat menurunkan tegangan permukaan serta meningkatkan karakteristik kinerja listrik dari divais terutama efek kanal melengkung dan efek pembawa panas. Oleh karena itu, MOSFET kanal yang berbelok mempunyai prospek aplikasi yang sangat besar didalam pembiatan arsitektur divais berukuran sangat kecil.
Kata kunci*: MOSFET, bukan planar, kanal melengkung, tegangan permukaan, efek kanal melengkung*

Introduction

In order to keep under control the short channel effects (SCEs), modifications of Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) structures have shown to be a good alternative to traditional bulk MOSFETs. New structure devices such as grooved-gate, recessed-channel, V-shaped and vertical MOSFET [1-4] (Fig. 1). Previous works have demonstrated that, in spite of their benefits, the MOSFET with curved-channel can reduce the Short Channel Effect. The presence of the groove in recessed-channel or grooved-gate MOSFETs can enhance the electrical performance [5]. The curved structure at the channel of device is effective in reducing the electric field at the drain, thus improving reliability. Furthermore, it can also reduce the substrate current, and increase the highest applicable gate to drain voltage, so that improving the reliability of the device. This phenomenon is the so called corner effects. It has been shown that corner effects are highly related to the geometrical parameters of the device, as long as to the doping density [5]. Previous works have focused on the influence of the corner effect that may affect the potential barriers for the device channel [6,7] which can improve the characteristics of the device especially the reduction of short channel effect (SCE) such as a high threshold voltage (V_{th}), a low DIBL and GIDL effect, closeness to ideal sub-threshold slope, and a high I_{ON}–I_{OFF} ratio [8-10].

Therefore, the main goal of this work is to carry out a thorough study of the corner effects for MOSFET which has curved-channel. To do so, we have developed a numerical simulator that self-consistently solves the Poisson equations in the structure under study. As it can be seen in Fig. 1, all device structures have the corner region in the channel, allowing a more effective control of the electrostatics in the channel.

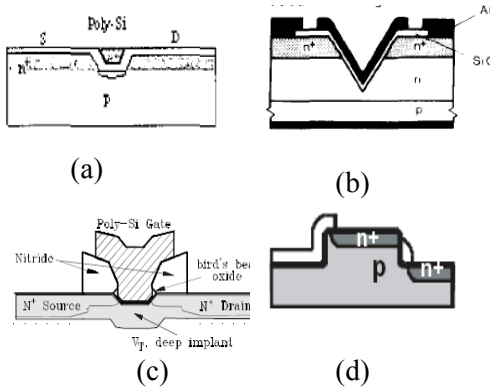

Figure 1. Some structures of MOSFETs with curved-channel such as structures of (a) Grooved-gate,(b) V-shaped, (c) recessed-channel (d) sidewall vertical

Method

The schematic cross-section diagram of this single gate vertical sidewall MOSFET depletion layer is shown in the Figure 2.

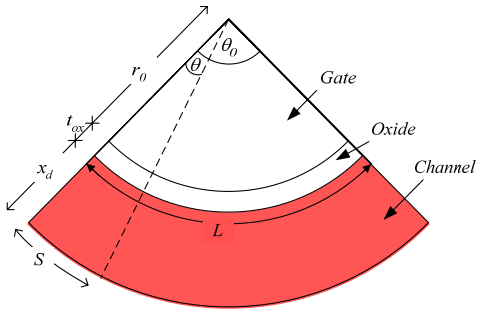

Figure 2. The aproximation of curved-channel MOSFET as cylindrical coordinates

This area is described by a quarter circles. For the simplified structure in Figure 2, the 2-D Poisson equation for these areas of the device can be given as follows [2,11] :

$$\frac{\partial^2\phi_2(r,\theta)}{\partial r^2}+\frac{1}{r}\frac{\partial\phi_2(r,\theta)}{\partial r}+\frac{1}{r^2}\frac{\partial^2\phi_2(r,\theta)}{\partial\theta^2}=\frac{qN_A}{\varepsilon_{Si}} \quad (1)$$

where ϕ is the electric potential in the active area of the device, ε_{Si} is the channel silicon permittivity, and N_A is the channel doping density. All the potentials of the device must consist of the same parameters, namely distances, so that for the curved-channel region, $\phi(r,\theta)$ can be converted into $\phi(s,r)$ where $s = r\,.\,\theta$.

The *s*-direction is considered along the channel length and *r*-direction along the depletion channel thickness. We assume that the concave corner is a part of the curved area and therefore the Poisson equation for the curve area potential uses cylindrical coordinates and the *s*-*r* coordinates. The potential distributions in the depletion layer for these areas are [2,11]:

$$\varphi(r,\theta)=\varphi_s(\theta)+D_1(\theta)r+D_2(\theta)r^2+D_3(\theta)r^3 \quad (2)$$

where L_p is the curved-channel length ($L_p = r\ \theta_0$)

The Poisson equation is solved separately for the three area regions using the following boundary conditions:

1. Potential at the depletion edge is given by :

$$\varphi(s,r_2)=\varphi_B \quad (3)$$

where ϕ_B is the body electrostatic potential and r_2 is position of the depletion edge, given as $r_2 = r_0+t_{ox}+w_d$.

2. Electric flux at the depletion edge is given by :

$$\left.\frac{\partial\varphi}{\partial r}\right|_{r=r_2}=0 \quad (4)$$

3. Electric flux at the interface of the gate/oxide is continuous for both the metal gates :

$$\left.\frac{\partial\varphi}{\partial r}\right|_{r=r_1} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\left[\frac{V_{gs}'-\varphi_{s2}[s]}{r_0\ln(1+t_{ox}/r_0)}\right] \quad (5)$$

where r_1 is position of the interface of the gate/oxide, $r_1 = r_0+t_{ox}$, ε_{ox} is the dielectric constant of the oxide, t_{ox} is the gate oxide thickness, V_{gs} is the gate-to-source bias voltage, $V_{gs}' = V_{GS}-V_{FB}$, V_{FB} being the flat band voltage. The gate oxide capacitance per unit area of flat region in the *x-y* direction and the pie-shaped region in the corner are listed in [2] as $C_r = \left(\frac{\varepsilon_{ox}}{r_0\ln(1+t_{ox}/r_0)}\right)$.

4. Potential at the source end is described as :

$$\varphi(x=0,y)=\varphi_{bi} \quad (6)$$

where $\phi_{bi} = (E_g/2) + V_T \ln (N_A N_D/n_i^2)$ is the built- in potential, N_D is the source/drain doping concentration, E_g is the silicon bandgap, V_T is the thermal voltage, and n_i is the intrinsic carrier concentration.

5. Potential at the drain end is described as :

$$\varphi(r,s=L)=V_{ds}+V_{bi}+V_{sub} \quad (7)$$

where L is channel length, $L=L_p$ and V_{DS} is the applied drain-source bias.

The values of the coefficients D_1 to D_3 in (2) can be calculated from the boundary conditions of 1 to 4.

We derived the equation for the surface potential from the Poisson equation [7] as shown here :

$$\frac{\partial^2\varphi_s(s)}{\partial s^2}-\alpha\varphi_s(s)=\beta \quad (8)$$

The α_i and β_i can be obtained by using boundary conditions at the source and drain.

$$\alpha = -\frac{6\,r_1\varepsilon_{Si}}{C_r r_1 r_2^2-(r_1-r_2)^2\varepsilon_{Si}}$$

$$\beta_2 = (r_1(C_r r_2^2(9r_1^2-8r_1r_2+r_2^2)(V_{gs}-1)-r_1(r_2-r_1)(N_a q r_2^2(r_2-3r_1)+ 6(r1-r2)\varepsilon_{Si}\phi_b)/(-C_r r_1(r_1-r_2)^2 r_2^2+(r_1-r_2)^4\varepsilon_{si})$$

The general solutions to confine the surface potential ϕ_s at the gate oxide/silicon interface are listed as :

$$\varphi_s(s) = A\exp(\eta s)+B\exp(-\eta s)-\frac{\beta}{\alpha} \quad (9)$$

where *A, B* are constants and $\eta = \sqrt{\alpha}$. Using boundary condition of 1-4, we can obtain coefficients of A and B.

Using surface potential equation from Eq. (8), we can derive the minimum surface potential φ_{smin} under condition $\left.\frac{\partial\varphi_s}{\partial\theta}\right|_{\theta=\theta_m}=0$, and obtain the angle when the minimum surface potential θ_m as

$$\theta_m = \frac{\lambda}{2}\ln\left(\frac{\Phi_s(e^{\frac{2\theta_0}{\lambda}}-1)-V_d}{\Phi_s(1-e^{-\frac{2\theta_0}{\lambda}})+V_d}\right) \quad (10)$$

Therefore, the minimum surface potential or the potential at θ_m is

$$\varphi_{smin} = V_g - \frac{N_A q x_d R_1}{C_{ox}(x_d-R_1)} + \frac{1}{2Sinh\left(\frac{2\theta_0}{\lambda}\right)}\sqrt{\left(\Phi_s\left(e^{\frac{2\theta_0}{\lambda}}-1\right)-V_d\right)\left(\Phi_s\left(1-e^{-\frac{2\theta_0}{\lambda}}\right)+V_d\right)} \quad (11)$$

Results and Discussion

Figure 3 also shows that no minimum potential point appears in the distribution line when the corner is smaller than a critical angle. This indicates that when the corner angle is too small, n potential barrier exists and the characteristics of the grooved-gate devices are analogous to that of the

planar ones. When it is bigger than the critical angle, the corner effect will be observed.

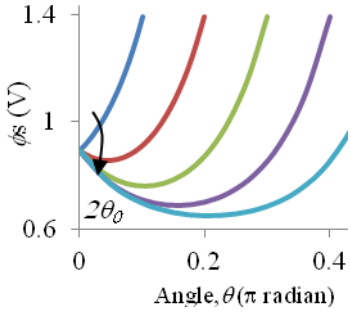

Figure 3. Surface potential distribution for different corner values

The corner effect of grooved-gate devices can be explained as follows : The smaller the radius of the corner, the more dispersive the electric field lines according to the theory of electric field. Because the radius of the planar part of the channel can be regarded as infinite, the electric field at the corner is very small, and the collapses of the surface potential form the barriers.

This minimum surface potential value shows the potential barrier height of the grooved gate device. These potential barrier height and minimum corner angle are shown in Fig 4 follows. From this graph, it shows that the minimum surface potential decrease with the increase of the corner angle, because the bigger the corner angle, the smaller the radius and the more heavily the surface potential collapses, giving rise to increase of the short channel effect.

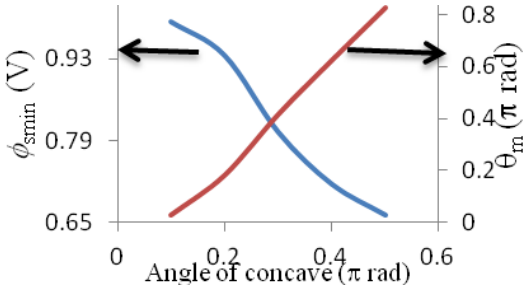

Figure 4. Formation of minimum surface potential and their respective position as a function of groove corner angle.

The parameter of λ describes the potential distribution in the depletion layer, which in turn depends on the device geometry and boundary conditions. Hence, to operate the device as in the long channel regime, i.e., to avoid the short channel effect, the minimum channel potential should be decreased by increasing the substrate doping concentration or by reducing λ. The definition of λ implies the bigger the corner angle θ_0, the smaller the radius r_0 and the smaller the λ , which is called the corner effect of grooved-gate MOSFET.

The theshold voltage (V_{th}) roll-of is shown in Fig. 5 below. The roll-off of V_{th} is suppressed in the grooved gate MOSFETs, a reverse short-channel effect is observed, where V_{th} becomes constant relatively, as the channel length is reduced. Further, the V_{th} value for groove channel MOSFET structure is found to be higher than planar MOSFET structure with the same substrate doping. This implies that the maximum barrier that electrons need to overcome when traveling from source to drain.

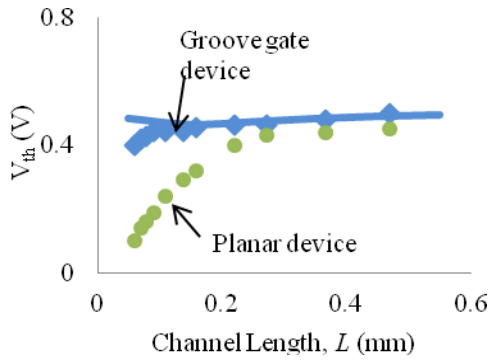

Figure 5. Threshold Voltage (V_{th}) roll-off of curved channel and planar MOSFETs for modeling (solid lines) and experiment (dot lines)

Conclusion

The electron potential profile in the channel region having concave corner, is derived by the Poisson equation in the cylindrical coordinates. This model studies the influence of the corner effect for the single gate vertical MOSFET. The electric field of the channel in the single gate vertical MOSFET and impact on the threshold are studied. The effects of corner effect on the Short Channel Effect (SCE) reduction of this device can easily be investigated using the simple model presented in this work. The emphasis of SCE is an advantage for the MOSFET structure with curved-channel as a candidate for small scale devices in the future.

The result shows that the minimum surface potential of a curved channel MOSFET is smaller than the planar MOSFET. Thus, the curved-channel MOSFET has a higher threshold voltage for various values of Lg'. The minimum surface potential of curved-channel MOSFET is higher than that of a planar MOSFET. The corner of channel has a "coupling" of the potential barriers, due to the potential barrier increase.

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